| L Number | Hits | Search Text | DB | Time stamp |
|---|---|---|---|---|
| 1 | 16 | ((data adj conversion) with (complet$3 or finish$3)) same updat$3 | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/12/29 07:18 |
| 2 | 3 | ((data adj conversion) with (complet$3 or finish$3)) same reload$3 | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/12/29 08:44 |
| 3 | 42 | ((data adj conversion) with (complet$3 or finish$3)) same (register$1) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/12/29 07:34 |
| 4 | 5 | 3.ti,ab,clm. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/12/29 07:22 |
| 5 | 13 | 341/$.ccls. and (((data adj conversion) with (complet$3 or finish$3)) same (register$1)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/12/29 07:22 |
| 6 | 1 | busy and (((data adj conversion) with (complet$3 or finish$3)) same (register$1)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/12/29 07:32 |
| 7 | 15 | ((data adj conversion) with (complet$3 or finish$3)) same busy | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/12/29 07:37 |
| 8 | 8 | latch$3 same (((data adj conversion) with (complet$3 or finish$3)) same (register$1)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/12/29 07:37 |
| 9 | 2 | (data adj conversion) with reload$3 | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/12/29 09:00 |
| 10 | 53 | (open adj drain$3) with delay | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/12/29 09:01 |
| 11 | 0 | (((data adj conversion) with (complet$3 or finish$3)) same updat$3) and ((open adj drain$3) with delay) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/12/29 09:01 |
| 12 | 0 | ((open adj drain$3) with delay) and (((data adj conversion) with (complet$3 or finish$3)) same (register$1)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/12/29 09:01 |

US-PAT-NO: 5347190

DOCUMENT-IDENTIFIER: US 5347190 A
**See image for Certificate of Correction**

TITLE: Magnetic bearing systems

DATE-ISSUED: September 13, 1994


INVENTOR-INFORMATION:

| NAME | CITY | STATE | ZIP CODE | COUNTRY |
|---|---|---|---|---|
| Lewis; David W. | Charlottesville | VA | N/A | N/A |
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US-CL-CURRENT: 310/90.5, 310/68B


ABSTRACT:

A magnetic bearing system includes a rotor with a plurality of masses distributed along the shaft including a portion having a circular peripheral surface suspended radially from pole pieces of permanent and electromagnets. A fault tolerant adaptive system responds to detected parameters of the rotor for varying the stiffness and damping the rotor. Position and speed of rotor are sampled at a rapid rate for each of a plurality of control axes and are processed independently during each sampling period. Malfunction of any of the processors causes supervisory controller to reconfigure the processing of the samples.


30 Claims, 37 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 24

---------- KWIC ---------

Detailed Description Text - DETX (81):

The serial input interface broadcasts the current analog-to-digital converter data to all DCM's in parallel with the actual conversion process itself. When an A/D conversion is started with the assertion of the ENCODE signal, the HAS-1204BM A/D converter begins its conversion sequence. This device is a **completely** self-contained **data conversion** system, including a high-speed track-and-hold amplifier, a 1.54 .mu.S 12 bit successive approximation A/D converter, and a timing generator. The complete sampling and conversion sequence requires a total of 2 .mu.S to complete. During the conversion, the A/D converter's serial data and clock inputs and the conversion complete signal are demultiplexed onto one of the SERIAL INPUT busses. These busses have been implemented with the user defined pins on the VME bus P2 connector. The output demultiplexers are implemented with five tri-state octal buffers, with one buffer per control channel. The three least significant bits

of control/status **register** 112 are decoded and used to activate one of the buffers. In this way, the CHAN field of CSR 112 directly controls which channel the DCM is controlling. Each DCM has ten 16 bit shift **registers** 118 to receive serial data broadcasts--five for the serial input bus and five for the serial output data bus. These shift **registers** are mapped into the CPU 88 I/O space. The shaft **registers** that have been chosen for this design include tri-state output **latches** for storing the contents of the shift **register** when the transmission has been completed. **Latching** of the shift **register** contents is initiated by the trailing edge of the A/D converter conversion complete signal, which is demultiplexed onto dedicated serial bus lines. Since the serial data for each channel are **latched** and presented to the CPU 88 only when the conversion is complete, the loose synchronization that is so important to this architecture is easily obtained.